a second phase-locked loop circuit configured to generate a second output signal phase-locked to the same reference clock signal; and

a frequency correction circuit configured to:

correct the first output signal by adjusting a first frequency-division ratio in the first phase-locked loop circuit in response to a detected frequency error in the first output signal;

calculate an adjustment parameter based on the detected frequency error; and

correct the second output signal by adjusting a second frequency-division ratio in the second phase-locked loop circuit, using the adjustment parameter.

10. The frequency synthesizer circuit of claim **9**, wherein the frequency correction circuit is configured to calculate the adjustment parameter based on an offset, so that the first and second output signal frequencies are corrected in different proportions.

11. The frequency synthesizer circuit of claim **10**, wherein the frequency correction circuit is configured to determine the offset based on a detected error in the second output signal.

12. The frequency synthesizer circuit of claim **10**, wherein the frequency correction circuit is configured to determine the offset based on a predicted error in the second output signal.

13. The frequency synthesizer circuit of claim **9**, wherein the frequency correction circuit is configured to schedule the adjustments of the first and second frequency-division ratios to avoid frequency discontinuities in the first or second output signals, or both, during one or more application-dependent time intervals.

14. A method for synthesizing two or more output signals from a reference clock signal, comprising:

generating a first output signal phase-locked to the reference clock signal, using a first phase-locked loop circuit;

generating a second output signal phase-locked to the reference clock signal, using a second phase-locked loop circuit;

correcting the first output signal by adjusting a first frequency-division ratio in the first phase-locked loop circuit and generating a control signal to adjust the frequency of the reference clock signal, in response to detected frequency error in the first output signal.

15. The method of claim **14**, wherein adjusting a first frequency-division ratio in the first phase-locked loop circuit comprises adjusting the first frequency-division ratio based on a Doppler shift resulting from motion relative to a remote transmitter.

16. The method of claim **14**, wherein generating the control signal comprises generating the control signal based on a reference frequency error in the reference clock signal.

17. The method of claim **14**, wherein generating the control signal comprises generating the control signal based on an average of the detected frequency error obtained over an averaging interval and wherein adjusting a first frequency-division ratio in the first phase-locked loop circuit comprises adjusting the first frequency-division ratio based on the difference between the average of the detected frequency error and the detected frequency error.

18. The method of claim **14**, further comprising calculating an adjustment parameter based on the detected frequency error in the first output signal and the adjustment to the reference clock frequency, and correcting the second output signal by adjusting a second frequency-division ratio in the second phase-locked loop circuit, using the adjustment parameter.

19. The method of claim **14**, further comprising scheduling the adjustments of the reference clock signal frequency and the first frequency-division ratio to avoid frequency discontinuities in the first or second output signals, or both, during one or more application-dependent time intervals.

20. A method for synthesizing two or more output signals from a reference clock signal, comprising:

generating a first output signal phase-locked to the reference clock signal, using a first phase-locked loop circuit;

generating a second output signal phase-locked to the reference clock signal, using a second phase-locked loop circuit;

correcting the first output signal by adjusting a first frequency-division ratio in the first phase-locked loop circuit in response to detected frequency error in the first output signal;

calculating an adjustment parameter based on the detected frequency error; and

correcting the second output signal separately from the correction to the first output signal by adjusting a second frequency-division ratio in the second phase-locked loop circuit, using the adjustment parameter.

21. The method of claim **20**, wherein calculating an adjustment parameter based on the detected frequency error comprises calculating the adjustment parameter based on an offset, so that the first and second output signal frequencies are corrected in different proportions.

22. The method of claim **20**, further comprising scheduling the adjustments of the first and second frequency-division ratios to avoid frequency discontinuities in the first or second output signals, or both, during one or more application-dependent time intervals.

23. A communications device, comprising

a communications transceiver circuit;

a second receiver circuit;

a first phase-locked loop circuit configured to generate a first output signal phase-locked to a reference clock signal, for use by the communications transceiver;

a second phase-locked loop circuit configured to generate a second output signal phase-locked to the same reference clock signal, for use by the second receiver circuit; and

a frequency correction circuit configured to correct the first output signal by adjusting a first frequency-division ratio in the first phase-locked loop circuit and generating a control signal to adjust the frequency of the reference clock signal, in response to a frequency error in the first output signal detected by the communications transceiver circuit.

24. The communications device of claim **23**, wherein the frequency correction circuit is further configured to calculate an adjustment parameter based on the detected frequency error and the adjustment to the reference clock frequency, and to correct the second output signal by adjusting a second frequency-division ratio in the second phase-locked loop circuit, using the adjustment parameter.

25. The communications device of claim **23**, wherein the frequency correction circuit is configured to schedule the adjustments of the reference clock signal frequency and the first frequency-division ratio to avoid frequency discontinuities in the first or second output signals, or both, during one or more application-dependent time intervals.

* * * * *